Docket No.: A0312.70412US00

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Rasekh Rifaat et al.

Serial No.:

09/925,889

Confirmation No.:

6192

Filed:

August 6, 2001

For:

DESPREAD SIGNAL RECOVERY IN DIGITAL SIGNAL

PROCESSORS

Examiner:

K. M. Burd

Art Unit:

2611

Certificate of Mailing Under 37 CFR 1.8(a)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: 12/04/07

COMMENTS ON THE STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

The Notice of Allowance mailed October 2, 2007 includes an Examiner's Statement Of Reasons For Allowance that describes the prior art (Lee EP 1 017 183) cited in the previous Office Action. The Examiner states that "Lee does not disclose each signal value comprises a real component and an imaginary component as stated in the amended claims." This does not accurately describe the teachings of Lee as Lee does disclose signal values comprising a real component and an imaginary component. Lee does not, however, teach, disclose, or suggest a single instruction, which specifies a plurality of signal values, each signal value having multiple real bits and multiple imaginary bits, and a plurality of code segments, and performs complex multiplication, addition and storing all within a single clock cycle as stated in the amended claims. If the Examiner disagrees, he is respectfully requested to contact Applicants' representatives so that the record can be made clear in this regard.

If there are any questions concerning the foregoing, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

By___

Ilan N. Barzilay

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Date: December 4, 2007